



Doc. Number:

- ☐ Tentative Specification
☐ Preliminary Specification
☒ Approval Specification

MODEL NO.: N173FGE
SUFFIX: LA3

Customer:**APPROVED BY****SIGNATURE****Name / Title**

Note

Please return 1 copy for your confirmation with your signature and comments.

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REVISION HISTORY

Version	Date	Page	Description
1.0	2012/4/16	All	Preliminary specification ver.1.0 was first issued.
2.0	2012/05/08	All	Approval specification ver.2.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N173FGE-LA3 is a 17.3" (17.3" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1600 x 900 HD+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	17.3 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1600 x R.G.B. x 900	pixel	-
Pixel Pitch	0.2388 (H) x 0.2388(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), AG	-	-
Luminance, White	220	Cd/m2	
Power Consumption	Total 5.74 W (Max.) @ cell 1.24 W (Max.), BL 4.5 W (Max.)		(1)

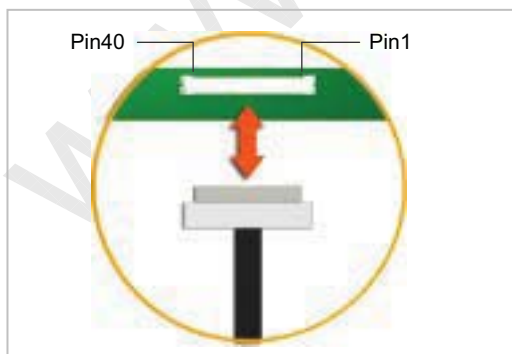
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, $f_v = 60$ Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and $T_a = 25 \pm 2$ °C, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	397.6	398.1	398.6	mm	(1)
	Vertical (V)	232.3	232.8	233.3	mm	
	Thickness (T)	-	5.5	5.8	mm	
Bezel Area	Horizontal	386.58	386.88	387.18	mm	
	Vertical	218.02	218.32	218.62	mm	
Active Area	Horizontal	-	382.08	-	mm	
	Vertical	-	214.92	-	mm	
Weight		-	530	545	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12 or equivalent

User's connector Part No: IPEX-20453-040T-01 or equivalent

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

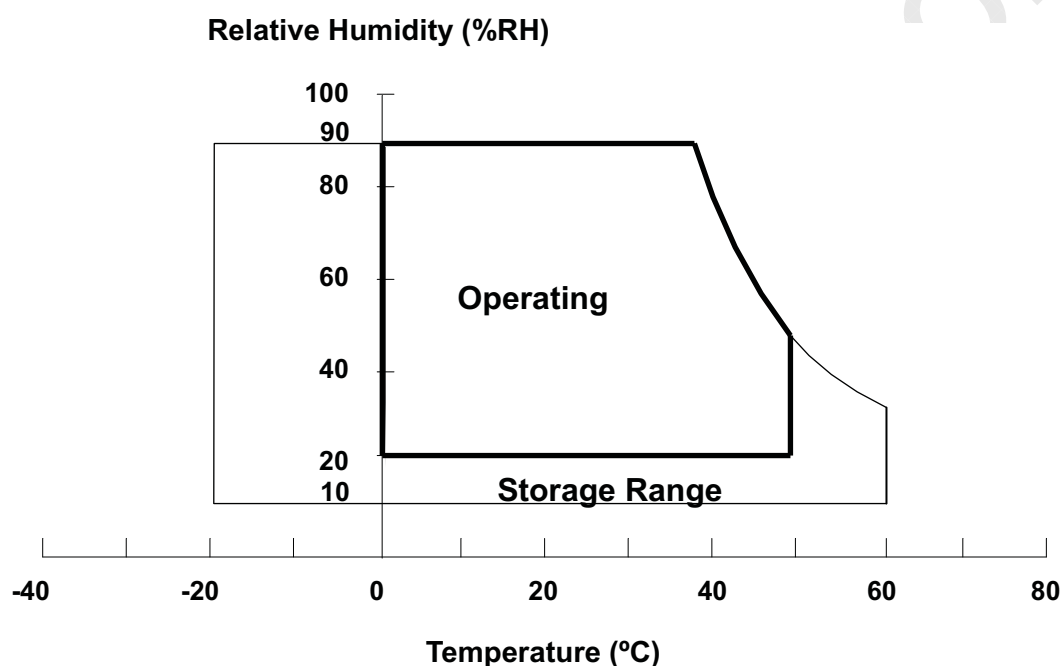
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. (Ta ≤ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



3.2 ELECTRICAL ABSOLUTE RATINGS

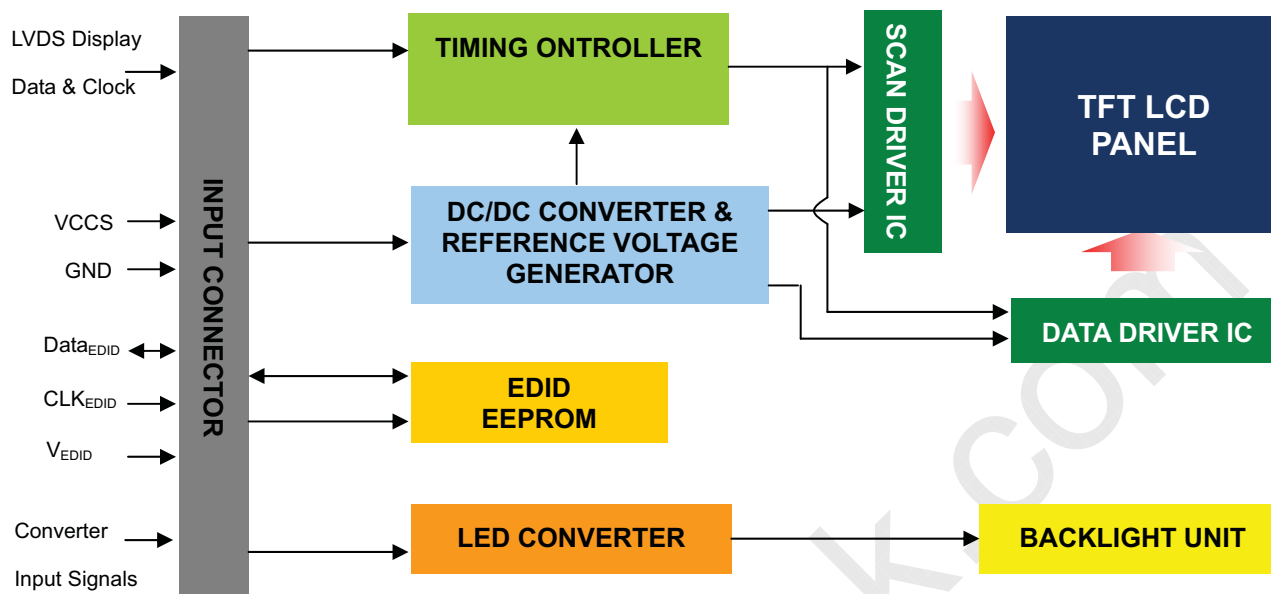
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	28	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5.5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5.5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS"..

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



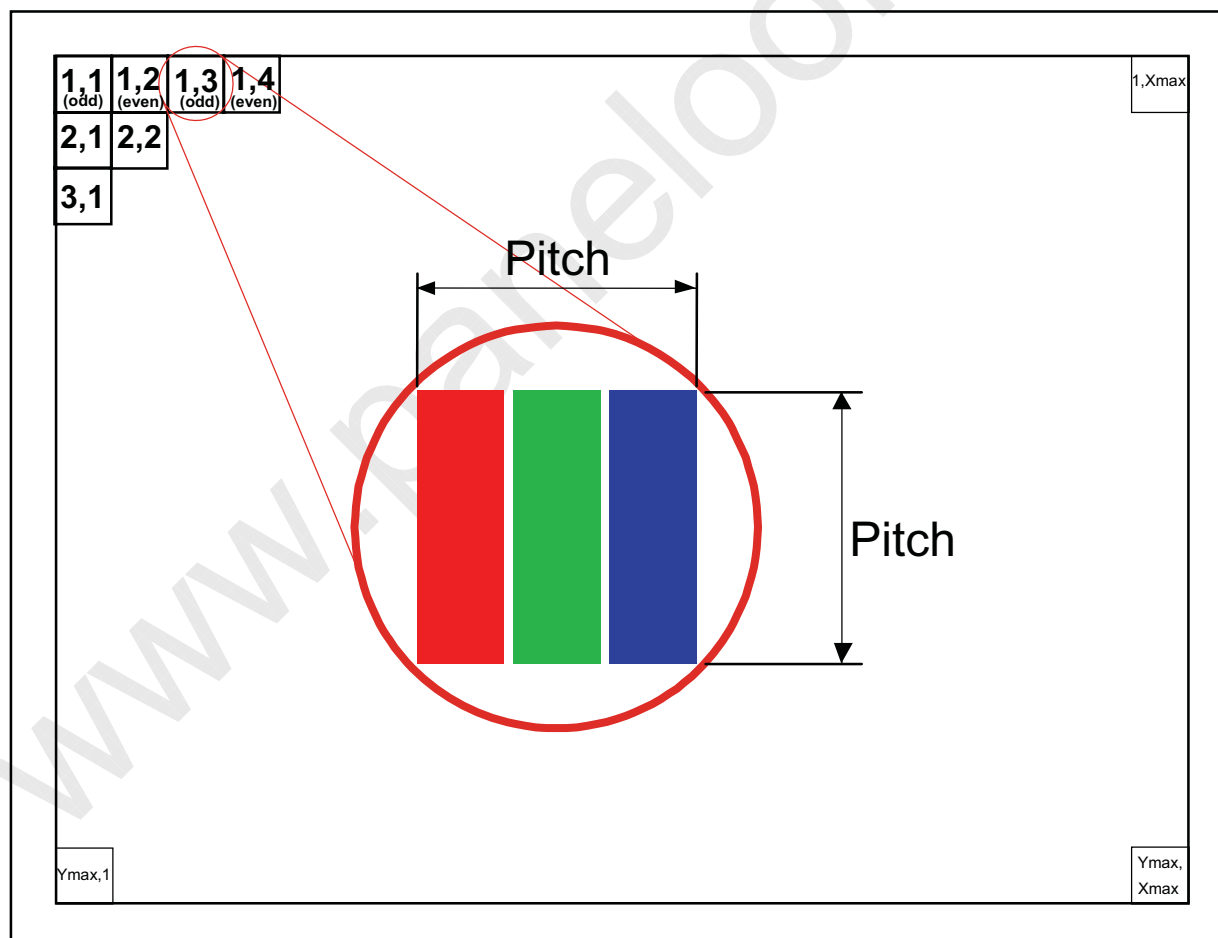
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	Loop or No Connection	
2	VCCS	Power Supply (3.3V typ.)	
3	VCCS	Power Supply (3.3V typ.)	
4	VEDID	DDC 3.3V power	
5	BIST	Panel self test	
6	CLKEDID	DDC clock	
7	DATAEDID	DDC data	
8	RXO0-	LVDS Differential Data Input (Odd)	R0-R5, G0
9	RXO0+	LVDS Differential Data Input (Odd)	
10	VSS	Ground	
11	RXO1-	LVDS Differential Data Input (Odd)	G1~G5, B0, B1
12	RXO1+	LVDS Differential Data Input (Odd)	
13	VSS	Ground	
14	RXO2-	LVDS Differential Data Input (Odd)	B2-B5,HS,VS, DE
15	RXO2+	LVDS Differential Data Input (Odd)	
16	VSS	Ground	
17	RXOC-	LVDS Clock Data Input (Odd)	LVDS CLK
18	RXOC+	LVDS Clock Data Input (Odd)	
19	VSS	Ground	
20	RXE0-	LVDS Differential Data Input (Even)	R0-R5, G0
21	RXE0+	LVDS Differential Data Input (Even)	
22	VSS	Ground	
23	RXE1-	LVDS Differential Data Input (Even)	G1~G5, B0, B1
24	RXE1+	LVDS Differential Data Input (Even)	

25	VSS	Ground	B2-B5,HS,VS, DE
26	RXE2-	LVDS Differential Data Input (Even)	
27	RXE2+	LVDS Differential Data Input (Even)	
28	VSS	Ground	LVDS CLK
29	RXEC-	LVDS Clock Data Input (Even)	
30	RXEC+	LVDS Clock Data Input (Even)	
31	LED_GND	LED Ground	
32	LED_GND	LED Ground	
33	LED_GND	LED Ground	
34	NC	Loop or No Connection	
35	LED_PWM	PWM Control Signal of LED Converter	
36	LED_EN	Enable Control Signal of LED Converter	
37	NC	No Connection (Reserve)	
38	LED_VCCS	LED Power Supply	
39	LED_VCCS	LED Power Supply	
40	LED_VCCS	LED Power Supply	

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

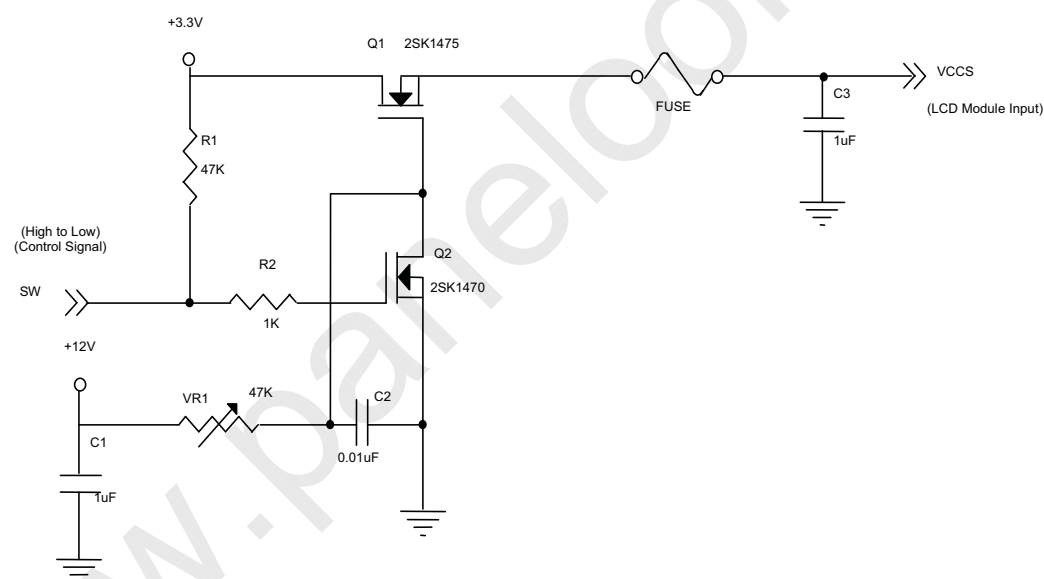
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
Ripple Voltage		V _{RP}	-	50	-	mV	(1)-
Inrush Current		I _{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I _{CC}	-	340	375	mA	(3)a
	Black		-	450	500	mA	(3)b
Power per EBL WG		P _{EBL}	-	2.315	-	W	(4)

Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

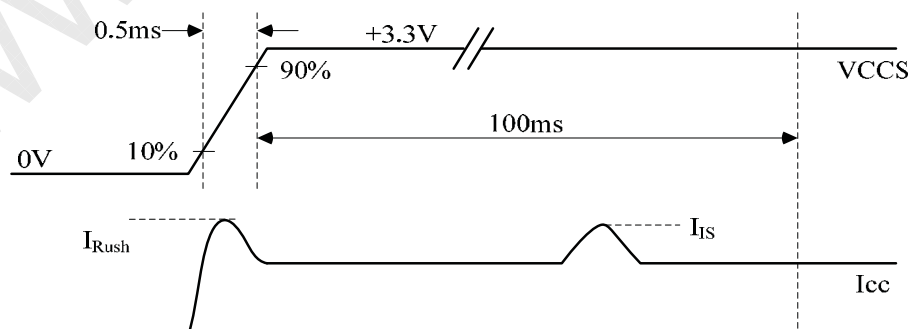
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

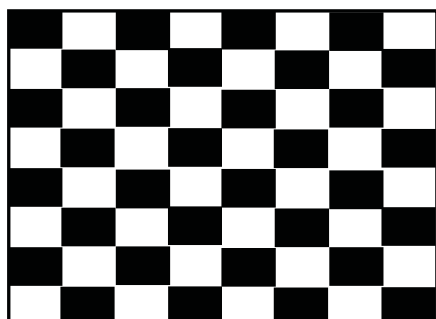


VCCS rising time is 0.5ms



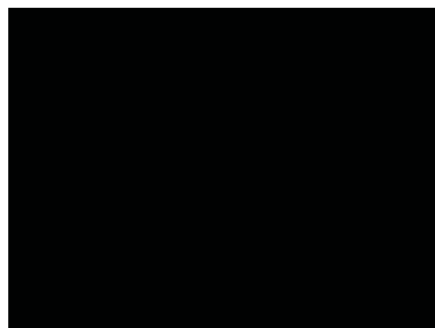
Note (3) The specified power supply current is under the conditions at $V_{CCS} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. Black Pattern



Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) $V_{CCS} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

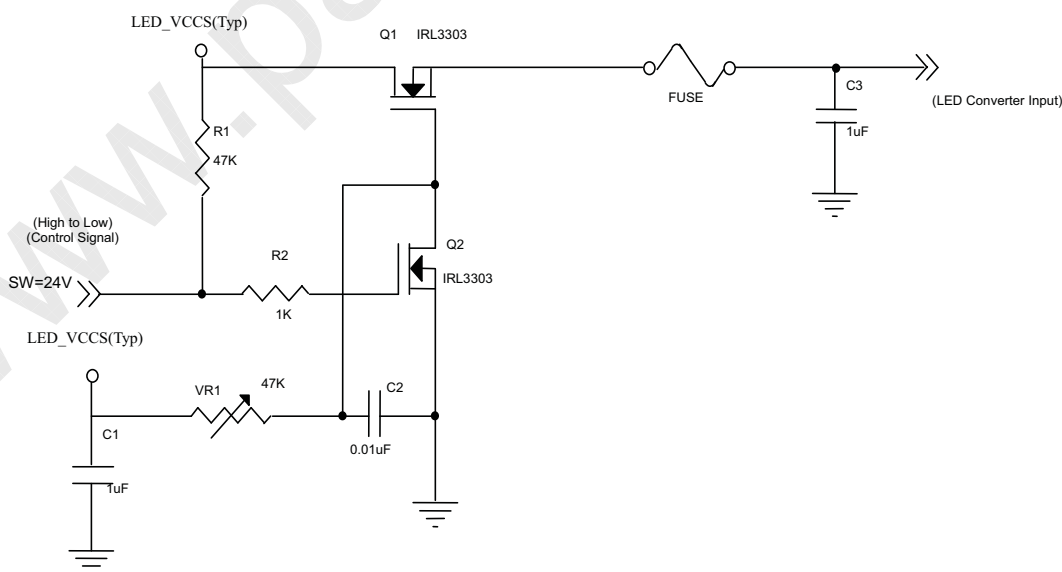
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	7.5	12	21	V	
Converter Inrush Current		I _{LED_{RUSH}}	-	-	1.5	A	(1)
EN Control Level	Backlight On		2	-	5	V	
	Backlight Off		0	-	0.8	V	
PWM Control Level	PWM High Level		2	-	5	V	
	PWM Low Level		0	-	0.15	V	
PWM Control Duty Ratio			10	-	100	%	
			5	-	100	%	(2)
PWM Control Permissive Ripple Voltage		V _{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f _{PWM}	190	-	1K	Hz	(3)
LED Power Current	LED_VCCS =Typ.	I _{LED}	277	364	375	mA	(4)

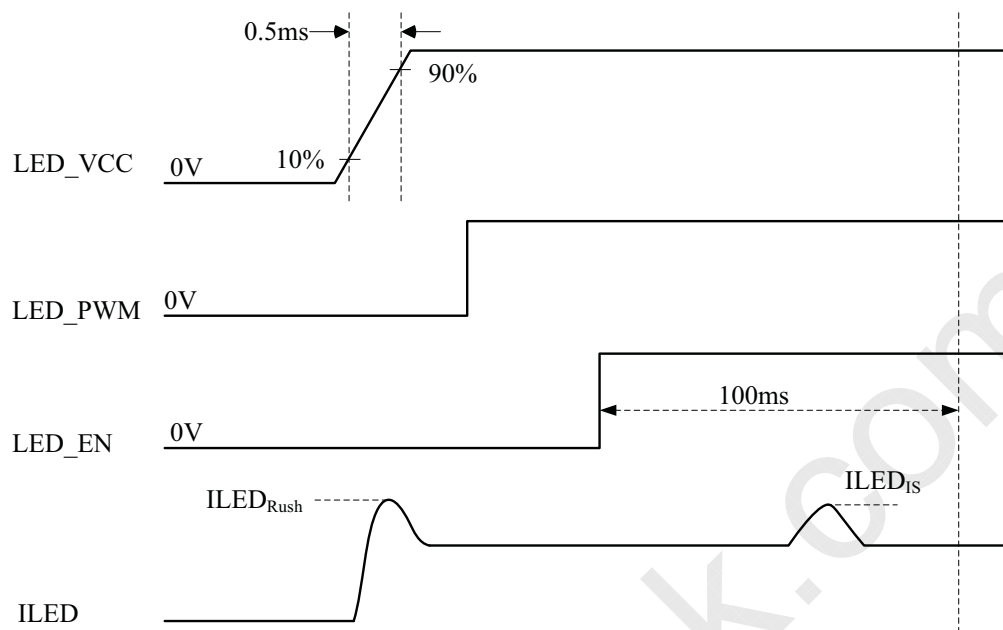
Note (1) I_{LED_{RUSH}}: the maximum current when LED_VCCS is rising,

I_{LED_{IS}}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If the PWM control duty ratio is less than 5%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer ($N \geq 3$)

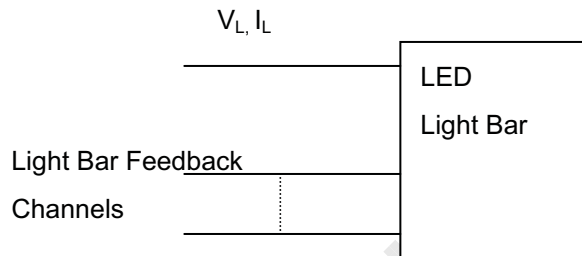
f : Frame rate

Note (4) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2^\circ\text{C}$, $f_{PWM} = 200\text{ Hz}$, Duty=100%.

4.3.3 BACKLIGHT UNIT $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	25.2	27.9	30.6	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L		125		mA	
Power Consumption	P_L		3.4875	3.825	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

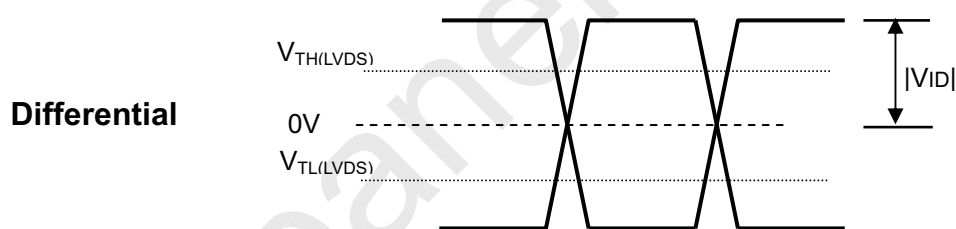
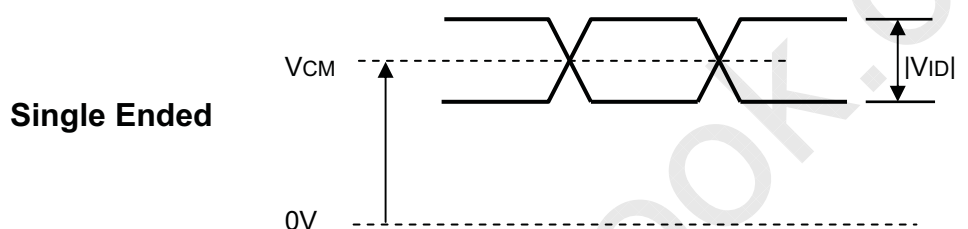
Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ and $I_L = 25\text{ mA(Per EA)}$ until the brightness becomes $\leq 50\%$ of its original value.

4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

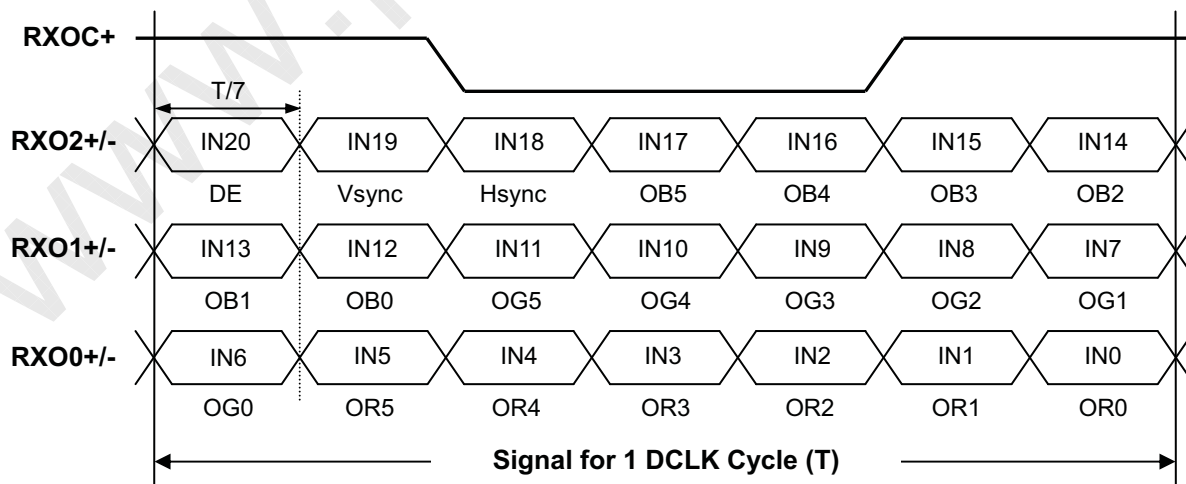
4.4.1 LVDS DC SPECIFICATIONS

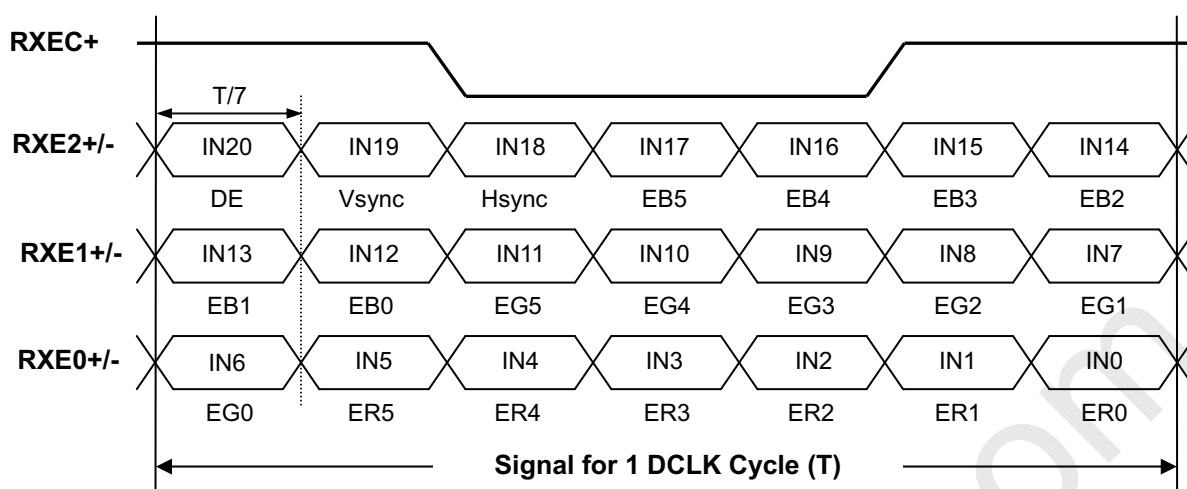
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), $V_{CM}=1.2V$
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1), $V_{CM}=1.2V$
LVDS Common Mode Voltage	V_{CM}	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	$ V_{ID} $	100	-	600	mV	(1)
LVDS Terminating Resistor	R_T	-	100	-	Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.



4.4.2 LVDS DATA FORMAT





4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

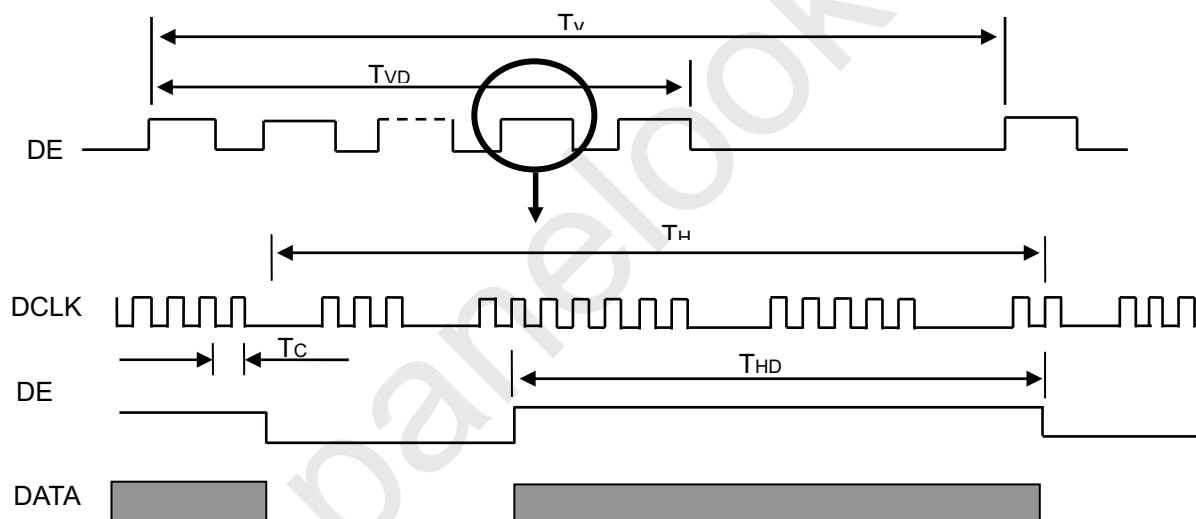
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	51.21	53.9	56.59	MHz	-
DE	Vertical Total Time	TV	907	926	932	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	-
	Horizontal Total Time	TH	1690	1940	2025	Tc	-
	Horizontal Active Display Period	THD	1600	1600	1600	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	340	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

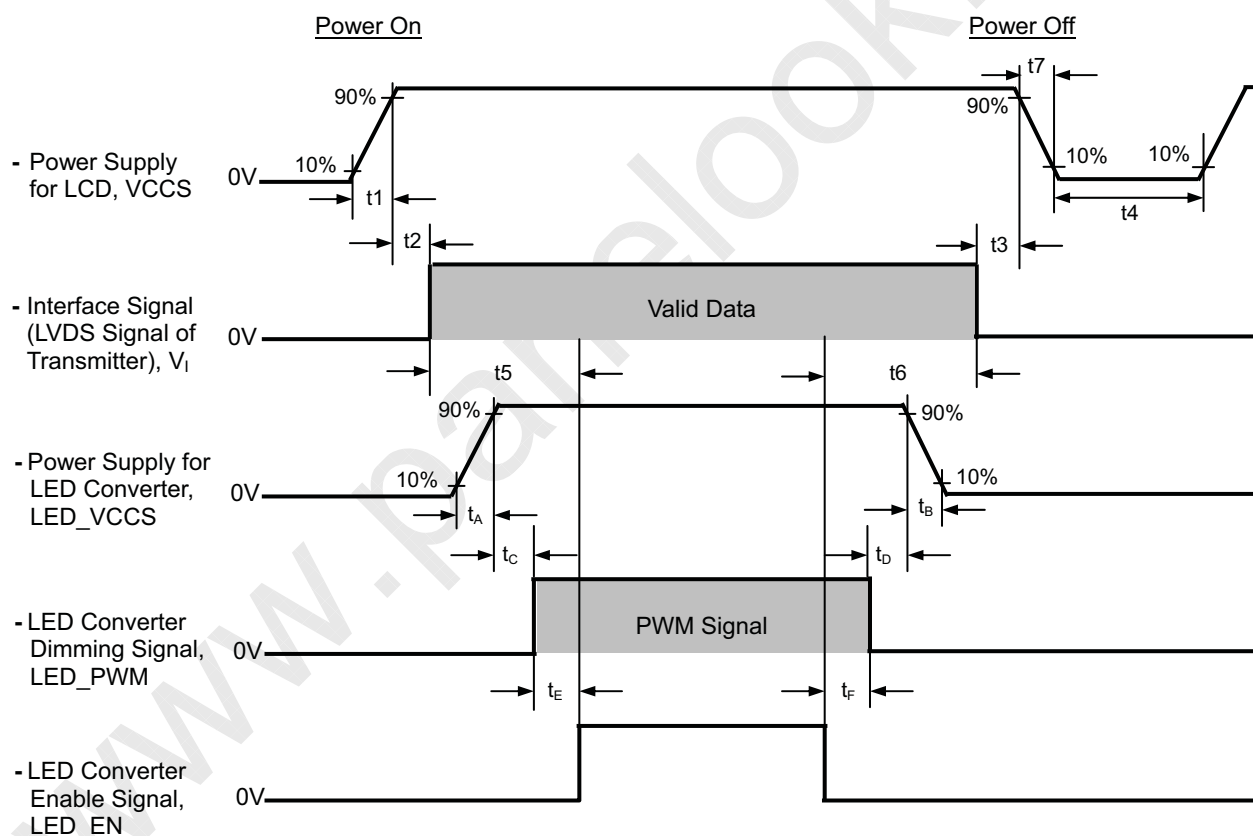
INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t1	0.5	-	10	ms	
t2	0	-	50	ms	
t3	0	-	50	ms	
t4	500	-	-	ms	
t5	200	-	-	ms	
t6	200	-	-	ms	
t7	0.5	-	10	ms	
t _A	0.5	-	10	ms	
t _B	0	-	10	ms	
t _C	10	-	-	ms	
t _D	10	-	-	ms	
t _E	10	-	-	ms	
t _F	10	-	-	ms	



Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

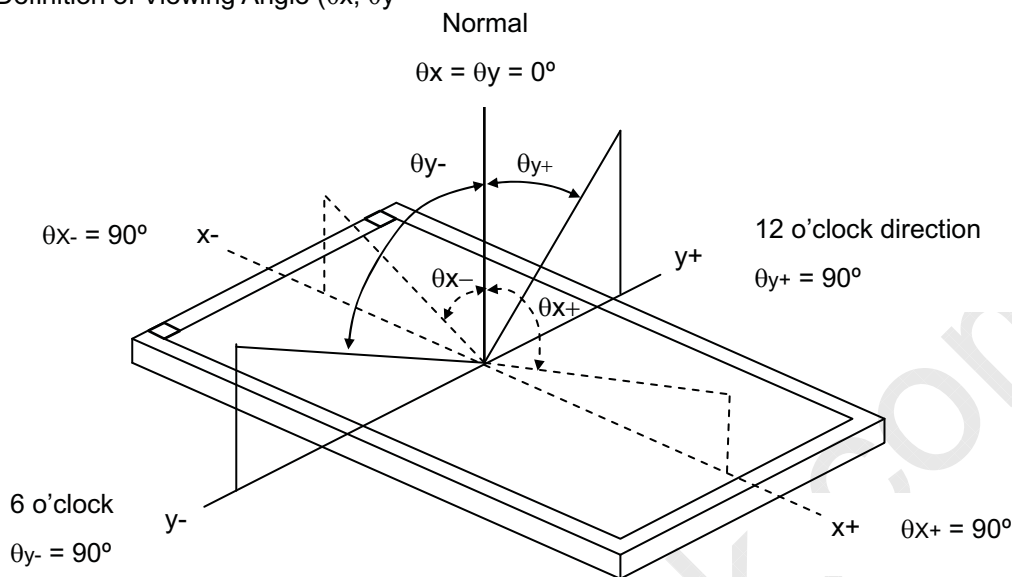
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	125	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	500	650	-	-	(2), (5) (7)
Response Time		T _R		-	3	8	ms	(3),(7)
		T _F		-	7	12	ms	
Average Luminance of White		L _{Ave}		185	220	-	cd/m ²	(4), (6) (7)
Color Chromaticity	Red	R _x		Typ – 0.03	0.617	Typ + 0.03	-	(1),(7)
		R _y			0.337		-	
	Green	G _x			0.342		-	
		G _y			0.588		-	
	Blue	B _x			0.156		-	
		B _y			0.074		-	
	White	W _x			0.313		-	
		W _y			0.329		-	
Viewing Angle	Horizontal	θ _x +	CR≥10	60	70	-	Deg.	(1),(5) (7)
		θ _x -		60	70			
	Vertical	θ _y +		50	60			
		θ _y -		50	60			
White Variation of 5 and 13 Points		δW _{5p}	θ _x =0°, θ _y =0°	80	-	-	%	(5),(6)
		δW _{13p}	θ _x =0°, θ _y =0°	-	-	-	%	(7)

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

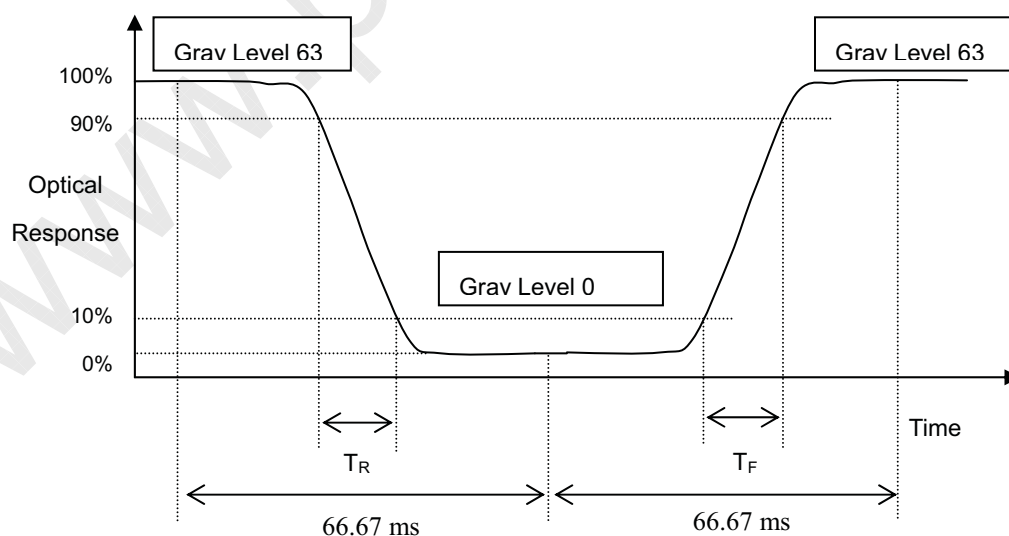
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$CR = CR(1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

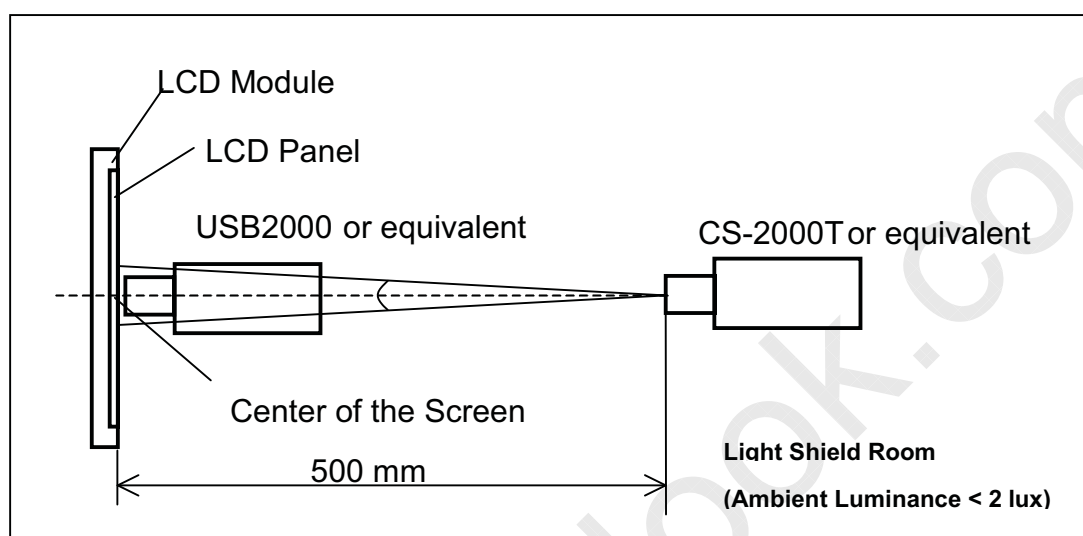
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

L(x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

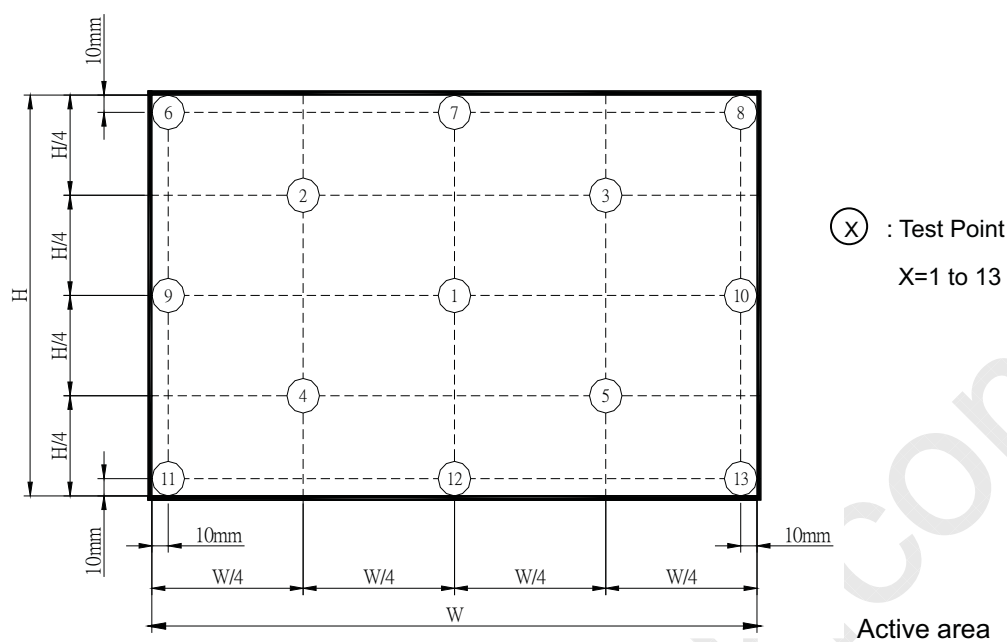


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W_{5p} = \{ \text{Minimum } [L(1) \sim L(5)] / \text{Maximum } [L(1) \sim L(5)] \} * 100\%$$

$$\delta W_{13p} = \{ \text{Minimum } [L(1) \sim L(5)] / \text{Maximum } [L(1) \sim L(5)] \} * 100\%$$



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour \longleftrightarrow 60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, RH 80%, 240hours	
ESD Test (Operation)	150pF, 330 Ω , 1sec/cycle Condition 1 : Contact Discharge, ± 8 KV Condition 2 : Air Discharge, ± 15 KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of $\pm X, \pm Y, \pm Z$	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

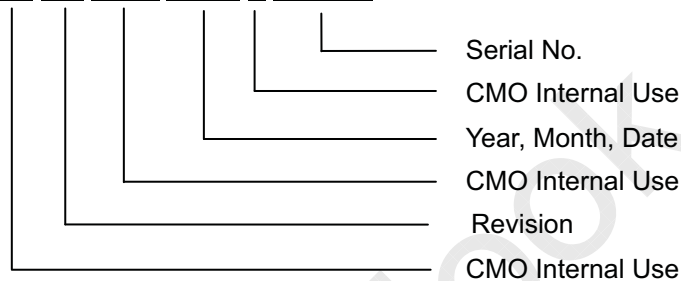
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N173FGE – LA3

(b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.

(c) Serial ID: XXXXXXXYMDLNNNN



(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL/CB logo: “AAAA” especially stands for panel manufactured by CMO Ningbo satisfying UL/CB requirement. “LEOO” is the CMO’s UL factory code for Ningbo factory.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

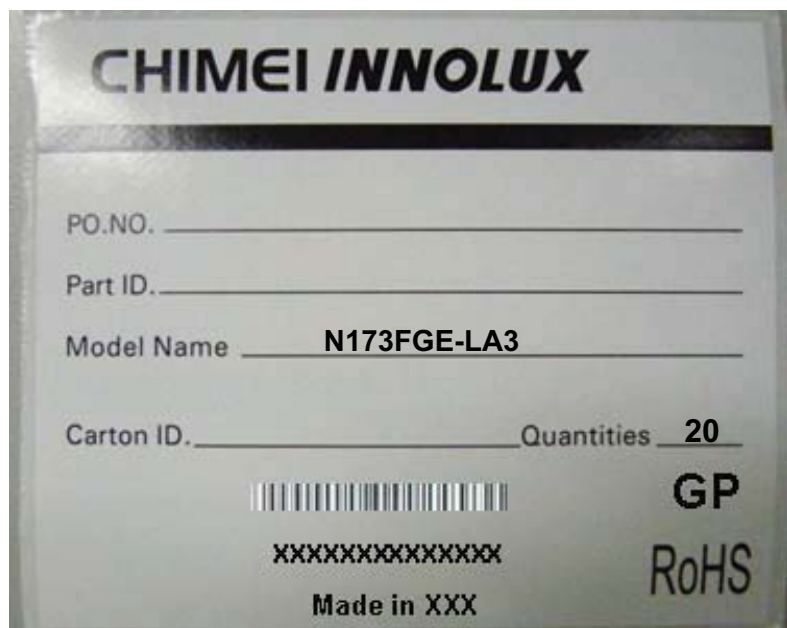
Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

HP CT label bar code definition: (Current version is CBANQ03K6WWXXX)

S/N	CT: CBSCPXXVRXXXXX
CT:	Title
C	LCD Display Module
BANQ	Assembly Code
03	Revision
K6	Supplier /Site of MFG
XX	Week/Year of MFG
XXX	Serial number. From 000000 to 999999

7.2 CMI Carton LABEL


CHIMEI INNOLUX

PO.NO. _____

Part ID. _____

Model Name **N173FGE-LA3**

Carton ID. _____ Quantities **20**



GP

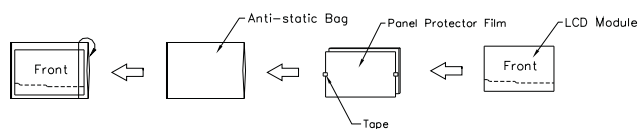
RoHS

XXXXXXXXXXXXXXXXXX

Made in XXX

(a) Production location: Made In XXXX. XXXX stands for production location.

7.3 CARTON



Box Dimensions : 490(L)*350(W)*320(H) mm
 Weight: Apprx. 13.6kg(20 module .per. 1box)

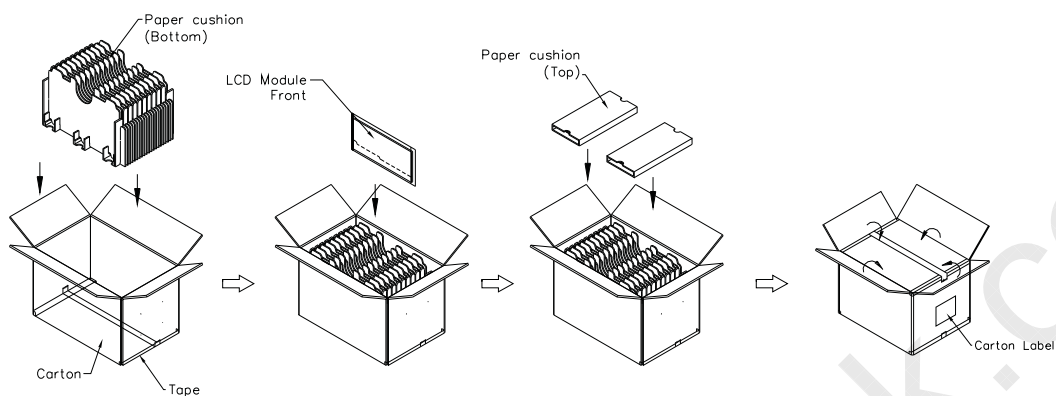
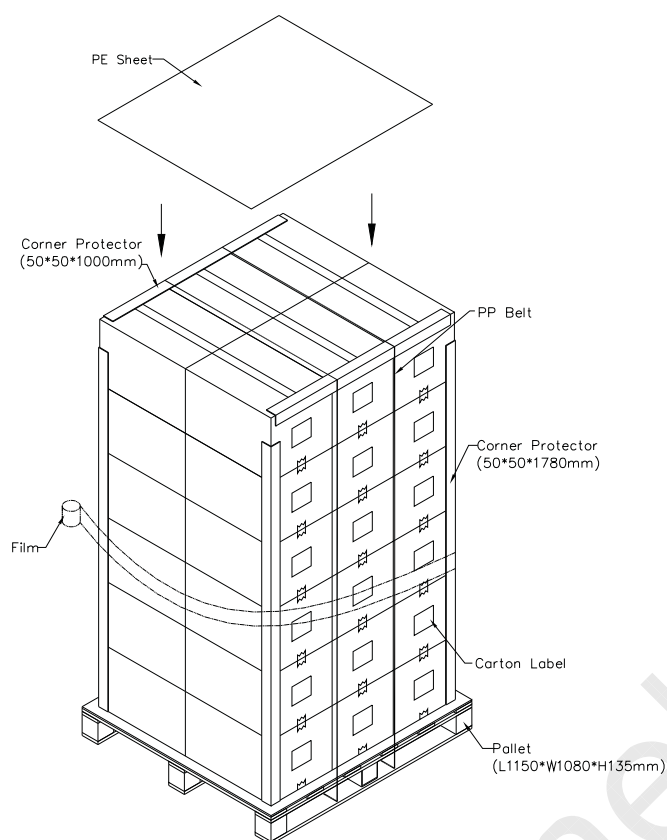


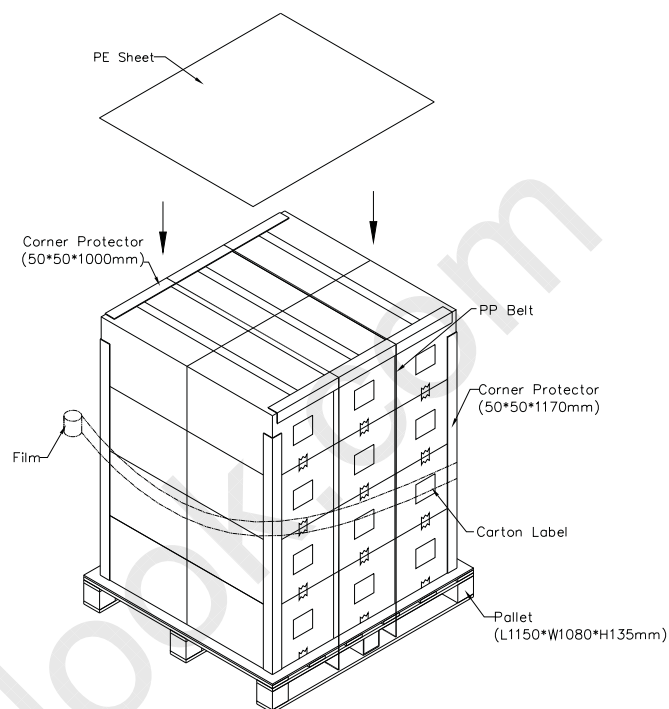
Figure. 7-3 Packing

7.4 PALLET

Sea & Land Transportation



Air Transportation

**Figure. 7-4 Packing**

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

**Appendix. EDID DATA STRUCTURE**

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMN")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AE	10101110
10	0A	ID product code (N173FGE-LA3)	32	00110010
11	0B	ID product code (hex LSB first; N173FGE-LA3)	17	00010111
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	01	00000001
17	11	Year of manufacture (fixed year code)	16	00010110
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("4")	04	00000100
20	14	Video I/P definition ("digital")	90	10010000
21	15	Max H image size ("38.768cm")	27	00100111
22	16	Max V image size ("21.852cm")	16	00010110
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	1A	00011010
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	05	00000101
27	1B	Rx=0.617	9E	10011110
28	1C	Ry=0.337	56	01010110
29	1D	Gx=0.342	57	01010111
30	1E	Gy=0.588	96	10010110
31	1F	Bx=0.156	28	00101000
32	20	By=0.074	13	00010011
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001

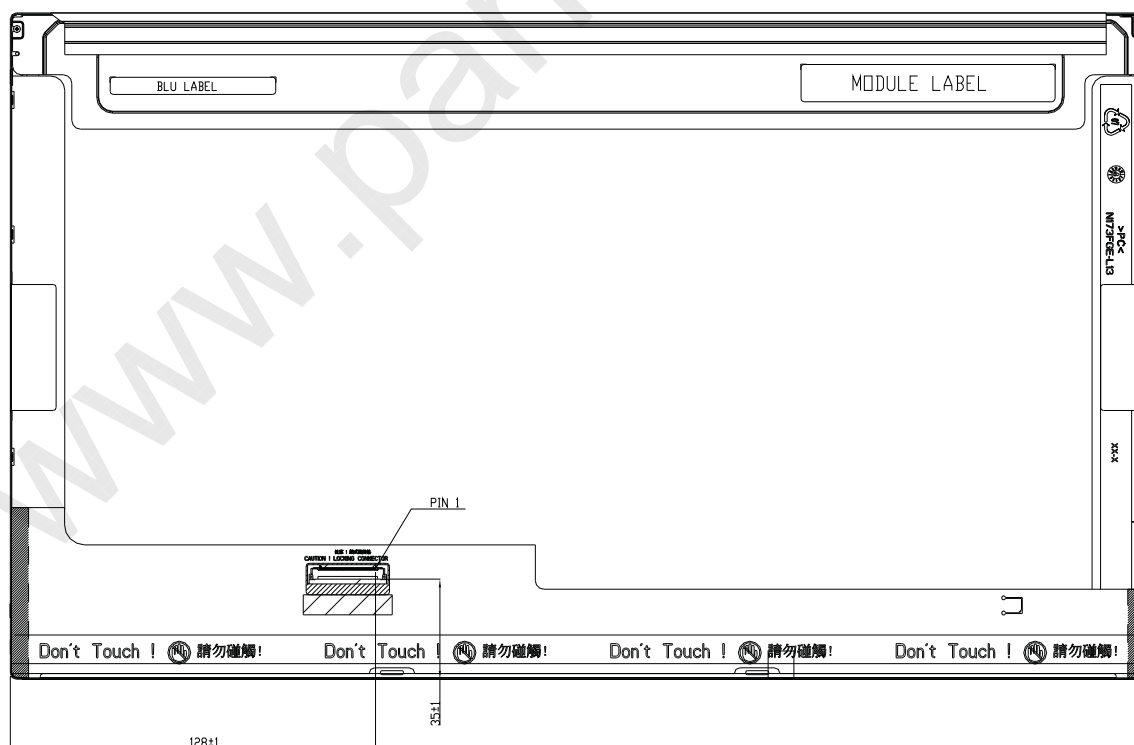
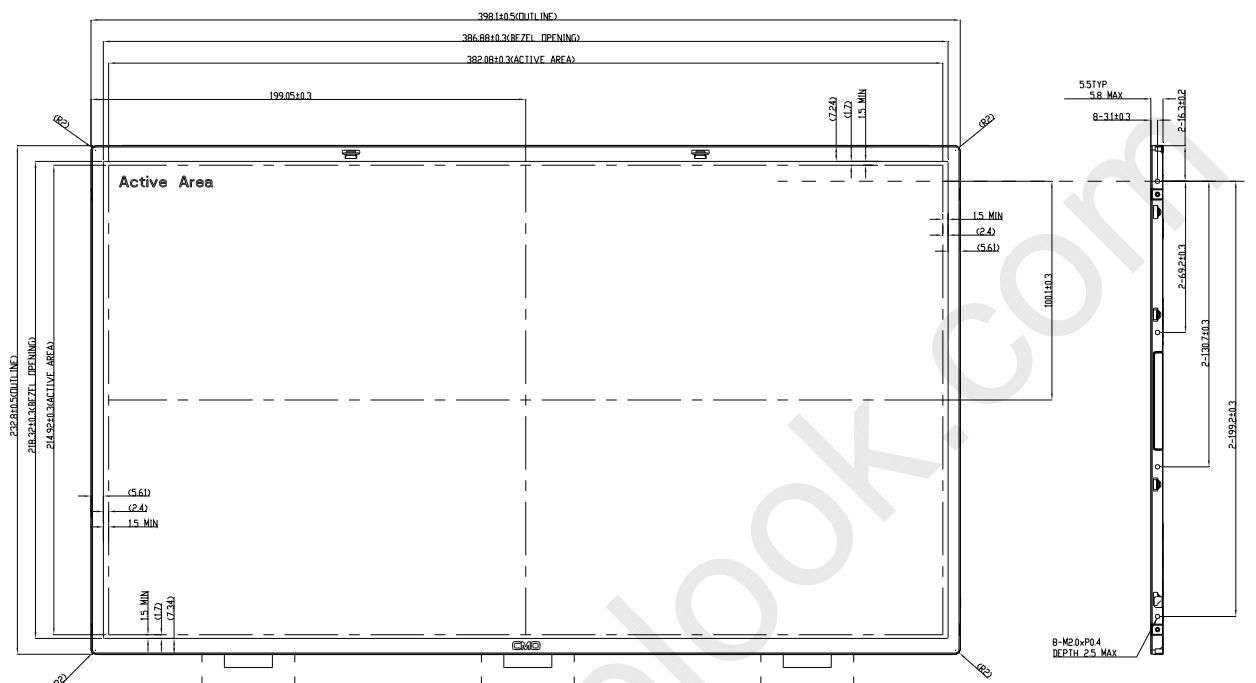


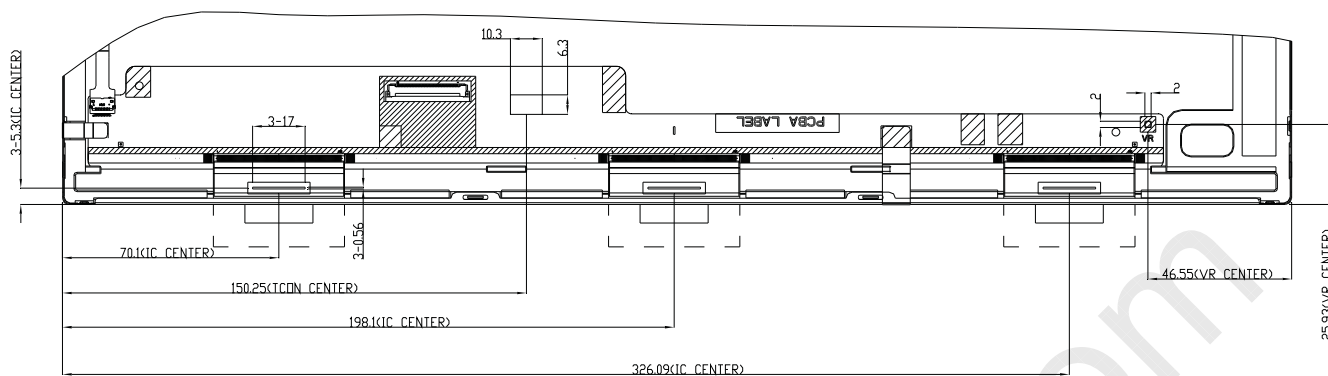
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("107.80MHz", According to VESA CVT rev1.1)	1C	00011100
55	37	# 1 Pixel clock (hex LSB first)	2A	00101010
56	38	# 1 H active ("1600")	40	01000000
57	39	# 1 H blank ("340")	54	01010100
58	3A	# 1 H active : H blank ("1600 : 340")	61	01100001
59	3B	# 1 V active ("900")	84	10000100
60	3C	# 1 V blank ("26")	1A	00011010
61	3D	# 1 V active : V blank ("900 : 26")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 5")	35	00110101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 5")	00	00000000
66	42	# 1 H image size ("382 mm")	7E	01111110
67	43	# 1 V image size ("215 mm")	D7	11010111
68	44	# 1 H image size : V image size ("382 : 215")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
72	48	Detailed timing description # 1 Pixel clock ("71.86MHz", According to VESA CVT rev1.1)	12	00010010
73	49	# 1 Pixel clock (hex LSB first)	1C	00011100
74	4A	# 2 H active ("1600")	40	01000000
75	4B	# 2 H blank ("340")	54	01010100
76	4C	# 2 H active : H blank ("1600 : 340")	61	01100001
77	4D	# 2 V active ("900")	84	10000100
78	4E	# 2 V blank ("26")	1A	00011010
79	4F	# 2 V active : V blank ("900 : 26")	30	00110000
80	50	# 2 H sync offset ("48")	30	00110000
81	51	# 2 H sync pulse width ("32")	20	00100000
82	52	# 2 V sync offset : V sync pulse width ("3 : 5")	35	00110101
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 5")	00	00000000



84	54	# 2 H image size ("382 mm")	7E	01111110
85	55	# 2 V image size ("215 mm")	D7	11010111
86	56	# 2 H image size : V image size ("382 : 215")	10	00010000
87	57	# 2 H boarder ("0")	00	00000000
88	58	# 2 V boarder ("0")	00	00000000
89	59	# 2 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
90	5A	NA	00	00000000
91	5B	NA	00	00000000
92	5C	NA	00	00000000
93	5D	NA	00	00000000
94	5E	NA	00	00000000
95	5F	NA	00	00000000
96	60	NA	00	00000000
97	61	NA	00	00000000
98	62	NA	00	00000000
99	63	NA	00	00000000
100	64	NA	00	00000000
101	65	NA	00	00000000
102	66	NA	00	00000000
103	67	NA	00	00000000
104	68	NA	00	00000000
105	69	NA	00	00000000
106	6A	NA	00	00000000
107	6B	NA	00	00000000
108	6C	Detailed Timing Description #4	00	00000000
109	6D	Flags	00	00000000
110	6E	Reserved	00	00000000
111	6F	For Brightness Table and Power Consumption	02	00000010
112	70	Flags	00	00000000
113	71	PWM % [7:0] @ Step 0 = 5 %	0C	00001100
114	72	PWM % [7:0] @ Step 5 = 27 %	44	01000100
115	73	PWM % [7:0] @ Step 10 = 91 %	E8	11101000
116	74	Nits [7:0] @ Step 0 = 10 nits	0A	00001010
117	75	Nits [7:0] @ Step 5 = 60 nits	3C	00111100
118	76	Nits [7:0] @ Step 10 = 200 nits	64	01100100
119	77	Panel Electronics Power @32x32 Chess Pattern = 1300 mW	20	00100000
120	78	Backlight Power @60 nits = 1000 mW	19	00011001
121	79	Backlight Power @Step 10 = 3333 mW	29	00101001
122	7A	Nits @ 100% PWM Duty = 220 nits	6E	01101110
123	7B	Flags	00	00000000
124	7C	Flags	00	00000000
125	7D	Flags	00	00000000
126	7E	Extension flag	00	00000000
127	7F	Checksum	F2	11110010

Appendix. OUTLINE DRAWING





DRIVER IC, CDF, TCON, AND VR LOCATIONS
SEE NOTES FOR EXPLANATION

General Tolerance Unless Specified				
0-3	±0.05	30-120	±0.15	1000-2000 ±0.5
3-6	±0.05	120-400	±0.2	2000-4000 -
6-30	±0.1	400-1000	±0.3	

NOTES :

1. MAX SCREW LENGTH : 2.5mm.
2. MAX SCREW TORQUE : 2.0 kgf-cm.
3. LCD MODULE INPUT CONNECTOR : I-PEX 20455-040E-12 OR FOXCONN GS13401-1110A-7H.
4. GAP BETWEEN BEZEL AND PANEL : 0.5mm MAX.
5. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER CDF, DRIVER IC, T-CON AND VR LOCATIONS.
6. LVDS CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
7. FLATNESS SPEC 0.5mm MAX.
8. 'C' MARKS THE REFERENCE DIMENSIONS.